What is claimed is:

1. A method of detecting a defect in a scan chain, the method comprising:

applying a plurality of pattern sets to a scan chain coupled to an array built-in self-test (ABIST) circuit;

collecting, from the scan chain, scan out data generated as a result of the application of the plurality of pattern sets to the scan chain; and

using the collected scan out data to identify a defective latch in the scan chain.

2. The method of claim 1, further comprising:

sensitizing at least one alternate path within which the scan chain is disposed; and

applying a second plurality of pattern sets to the scan chain while the alternate path is sensitized.

3. The method of claim 1, wherein using the collected scan out data to identify the defective latch includes identifying a location of the defective latch in the scan chain.

4. The method of claim 1, further comprising performing at least one of a scan test and a flush test prior to applying the plurality of pattern sets to the scan chain.

5. The method of claim 1, wherein applying the plurality of pattern sets includes laterally inserting each pattern set into the scan chain using the ABIST circuit.

6. The method of claim 1, wherein collecting the scan out data includes serially stepping the scan out data through the scan chain to an output thereof.

7. The method of claim 1, further comprising reconfiguring the scan chain prior to collecting the scan out data.

8. An apparatus, comprising:

a memory; and

program code resident in the memory and configured to detect a defect in a scan chain disposed in an integrated circuit device by collecting, from the scan chain, scan out data generated as a result of an application of a plurality of pattern sets to the scan chain by an array built-in self-test (ABIST) circuit disposed in the integrated circuit device, and using the collected scan out data to identify a defective latch in the scan chain.

9. The apparatus of claim 8, wherein the program code is further configured to sensitize at least one alternate path within which the scan chain is disposed, and apply a second plurality of pattern sets to the scan chain while the alternate path is sensitized.

10. The apparatus of claim 8, wherein the program code is configured to use the collected scan out data to identify the defective latch by identifying a location of the defective latch in the scan chain.

11. The apparatus of claim 8, wherein the program code is further configured to perform at least one of a scan test and a flush test prior to applying the plurality of pattern sets to the scan chain.

12. The apparatus of claim 8, wherein the program code is configured to apply the plurality of pattern sets by laterally inserting each pattern set into the scan chain using the ABIST circuit.

13. The apparatus of claim 8, wherein the program code is configured to collect the scan out data by serially stepping the scan out data through the scan chain to an output thereof.

14. The apparatus of claim 8, wherein the program code is further configured to reconfigure the scan chain prior to collecting the scan out data.

15. The apparatus of claim 8, wherein at least a portion of the program code is resident in a test platform.

16. The apparatus of claim 15, wherein at least a second portion of the program code is resident in computer coupled to the test platform.

17. A program product, comprising:

program code configured to detect a defect in a scan chain disposed in an integrated circuit device by collecting, from the scan chain, scan out data generated as a result of an application of a plurality of pattern sets to the scan chain by an array built-in self-test (ABIST) circuit disposed in the integrated circuit device, and using the collected scan out data to identify a defective latch in the scan chain; and

a computer readable signal bearing medium bearing the program code.

18. The program product of claim 17, wherein the computer readable signal bearing medium includes at least one of a transmission medium and a recordable medium.